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09/715,081	11/20/2000	Akitaka Nakayama	001542	7823

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EXAMINER	
SHAPIRO, JEFFERY A	

ART UNIT	PAPER NUMBER
3653	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/715,081	NAKAYAMA ET AL.	
	Examin r	Art Unit	
	Jeffrey A. Shapiro	3653	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear what a "fractional printed circuit board" is. Is it a remainder of a group not able to be placed on a sheet or is it a portion of one board?

Also, it is unclear what a detecting unit is. Is it a physical sensor or is it a portion of a software program which determines what the status of a group of printed circuit boards, for example?

Finally, Is it true that a determining unit is a judgement section of the program that judges the viability of a combination of printed circuit boards fitting on a particular sheet of material?

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Kalagnanam et al (US 6,044,361). Kitamura discloses the manufacturing system for printed wiring boards as follows.

As described in Claims 1, 9 and 10;

a. a schedule data storage unit (302) storing multiple manufacturing scheduling data including the kind of a printed wiring board scheduled to be manufactured and manufacturing quantity thereof;

b. a detecting unit (205) detecting a quantity of printed wiring boards which should be laid out in a single predetermined manufacturing block together with printed wiring boards of a different kind from multiple kinds of the printed wiring boards scheduled to be manufactured, according to multiple manufacturing schedule data; (Note that the system of Kitamura detects how much of a certain product exist in the system and determines how this product should be distributed or "laid out" in a single predetermined manufacturing block (a certain processing equipment). Note also figure 11, in which product information (1103), equipment information (1104) and a manufacturing situation (1105) are stored in memory and that network (1108) is connected to processing equipment (1110). See col. 8, lines 36-67. *The system of Kitamura, at the very least, implies that detection is occurring, otherwise, the system would not operate.*)

c. a condition data storage unit (204) storing a manufacturing condition data for laying out the printed wiring boards of different kinds in a single predetermined manufacturing block; (Note that laying out different wiring boards of different types is construed as placing them in a particular area of, for example, a component assembly machine, such that they will

be assembled. Note also col. 5, lines 36-55, which indicates that a designer inputs product information and related processing information. See also col. 5, lines 31-35. Note also col. 1, lines 7-16, which indicates that this designing concerns a semiconductor device and a process procedure. Such a device could be construed as requiring several printed wiring boards and the associated design data input by the designer can be construed to be information on where the machine will place various electronic components on said board. Even if this is not the case, it appears that it would be an obvious substitution to adapt such a computer based manufacturing system to integrate a printed circuit wiring board design operation with an associated assembly or fabrication process.)

d. a dividing unit dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data; (Note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information. Note also that such a system as described by Kitamura would necessarily be expected to group particular product based on a wide variety of criteria, including the particular process required, the particular model of board, as well as the manufacturing load on a particular piece of equipment. See col. 9, lines 22-27, for example.)

e. a determining unit determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group. (Note that the central processor (1101) necessarily divides detected quantities of product into efficient lot sizes for a particular piece of processing equipment based on the product information, the equipment information and process information. Note also that a determining unit can be construed to be a number of components of the system of Kitamura. For example, as described above, the system identifies the condition of a particular piece of equipment as well as how many items individually or in lots are being produced at which piece of equipment. The system of Kitamura necessarily must detect information about the manufacturing process through a particular means, otherwise, it would not work. See also col. 5, lines 12-27, as well as figures 11-13. Note element 1304 in figure 13, which "verifies the process procedure".)

As described in Claim 2;

f. said detecting unit, if a manufacturing quantity of the boards of a certain kind cannot be divided completely by a maximum number of the boards which can be laid out in a single predetermined manufacturing block, detects printed wiring boards corresponding to a number smaller than said maximum number or an excess of boards of said fraction. (Again, note that such a system as that of Kitamura necessarily maximizes

the most product that can fit on a particular machine so as to efficiently process the required product as determined by customer orders. As described above, the system of Kitamura necessarily describes load balancing of various production machines, and would not work otherwise in such an environment.)

As described in Claim 3;

g. the manufacturing condition data is data produced by combining orders with product data (note that customer orders and product data are necessarily combined in order to move material through the system—see also manufacturing situation memory (1105) and product information memory (1103), which are both used to optimize work flow through the production line);

As described in Claim 4;

h. the order data includes a shipment date (note that it is inherent and obvious that product moving through the system would have a shipment date assigned to it);

As described in Claims 5 and 6;

i. the product data includes the number of layers of the printed wiring boards (note that it would be obvious to include the number of layers as design and processing parameters since the process of Kitamura is for semiconductor manufacturing—see abstract, lines 1 and 2);

Kitamura does not expressly disclose handling fractional printed circuit boards or fractional groups of printed circuit boards.

Kalagnanam et al discloses handling fractional items in a manufacturing system with inventory matching. See col. 1, lines 48-67, col. 2, lines 1-67, col. 3, lines 1-67, col. 4, lines 1-67, and col. 5, lines 1-41.

Both Kitamura and Kalagnanam et al are analgous art because they both concern manufacturing inventory and scheduling.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the optimization routines of Kalagnanam et al in the system of Kitamura to identify and match partial items, such as printed circuit boards or partial lots/groups of printed circuit boards with orders or other requirements.

The suggestion/motivation would have been to reduce waste of PC-Boards. See Kalagnanam et al, col. 2, lines 33-37.

Therefore, it would have been obvious to combine Kitamura and Shin et al in order to obtain the invention as specified in Claims 7 and 8.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Kalagnanam et al and further in view of Shin et al. Kitamura discloses the system as described above. Kitamura does not expressly disclose, but Shin et al discloses the following.

As described in Claim 7;

j. a CAD data creating unit (see col. 17, lines 21-23) creating CAD data corresponding to a combination determined by said determining unit;

k. a CAD data converting unit creating CAM data or CAT data corresponding to CAD data created by said CAD data creating unit (see col. 17, lines 21-47);

As described in Claim 8;

l. a manufacturing unit group (20, 22, 24, 26 and 28) carrying out a manufacturing process for the printed wiring board using the CAM data or the CAT data created by said CAD data creating unit;

Both Kitamura and Shin et al are analgous art because they both concern manufacturing pc-boards.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the CAD and CAT creating units and converting units to create product and test data, as described by Shin et al, for use by the system of Kitamura.

The suggestion/motivation would have been to provide direct input of product information required for production and testing of PC-Boards.

Therefore, it would have been obvious to combine Kitamura and Shin et al in order to obtain the invention as specified in Claims 7 and 8.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dighe et al (US 5,815,398) in view of Kitamura. Dighe et al discloses the manufacturing system for placing groups of items to be cut out of sheet material on layouts, minimizing waste, as follows.

As described in Claim 1;

m. a detecting unit (59, 61) detecting a quantity of printed wiring boards (see col. 4, lines 62-65) which should be laid out in a single predetermined manufacturing block (54) together with printed wiring boards of a different kind from multiple kinds of the printed wiring boards scheduled to be manufactured, according to multiple manufacturing data;

n. a condition data storage unit (14, 16 and 18) storing a manufacturing condition data for laying out the printed wiring boards of different kinds in a single predetermined manufacturing block;

o. a dividing unit (44) dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data; (See col. 7, lines 28-44.)

p. a determining unit (20) determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group. (see col. 7, lines 45-65 and col. 8, lines 1-58.)

Dighe does not expressly disclose, but Kitamura discloses the following.

As described in Claim 1;

q. a schedule data storage unit storing multiple manufacturing scheduling data including the kind of a printed wiring board scheduled to be manufactured and manufacturing quantity thereof;

(Note that the system of Kitamura detects how much of a certain product exist in the system and determines how this product should be distributed or "laid out" in a single predetermined manufacturing block (a certain processing equipment). Note also figure 11, in which product information (1103), equipment information (1104) and a manufacturing situation (1105) are stored in memory and that network (1108) is connected to processing equipment (1110). See col. 8, lines 36-67. *The system of Kitamura, at the very least, implies that detection is occurring, otherwise, the system would not operate.*)

Both Dighe and Kitamura are considered to be analogous art because Dighe concerns a manufacturing process for cutting printed circuit boards and the like, and Kitamura concerns a manufacturing scheduling system for printed circuit board production systems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the scheduling system of Kitamura with the production cutting placement system of Dighe so as to schedule parts for placement on sheets of material.

The suggestion/motivation would have been to schedule orders concerning cutting processes for printed circuit boards and verifying their completion. See abstract of Kitamura and Dighe, abstract, col. 4, lines 55-67 and col. 5, lines 1-5 and 44-48, noting that Kitamura's system can be construed as teaching one type of algorithm for placing parts.

Note further, that should parts of a particular group not fit on a single sheet, that it would have been obvious to place them on a further sheet that fit the part.

Therefore, it would have been obvious to combine Kitamura and Dighe in order to obtain the invention as described in Claim 1.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blaimschein (US 5,953,232) in view of Kitamura. Blaimschein discloses the manufacturing system for placing groups of items to be cut out of sheet material on layouts, minimizing waste, as follows.

As described in Claim 1;

m. a detecting unit (3) detecting a quantity of printed wiring boards (see part e of Blaimschein's claim 1) which should be laid out in a single predetermined manufacturing block together with printed wiring boards of a different kind from multiple kinds of the printed wiring boards scheduled to be manufactured, according to multiple manufacturing data;

n. a condition data storage unit (10) storing a manufacturing condition data for laying out the printed wiring boards of different kinds in a single predetermined manufacturing block;

o. a dividing unit dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data; (Note that the items are placed on available pieces of sheet, as can fit—see Blaimschein's Claim 1.)

p. a determining unit determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group. (Again, see Blaimshein's Claim 1, for example.)

Blaimschein does not expressly disclose, but Kitamura discloses the following. As described in Claim 1;

q. a schedule data storage unit storing multiple manufacturing scheduling data including the kind of a printed wiring board scheduled to be manufactured and manufacturing quantity thereof;

(Note that the system of Kitamura detects how much of a certain product exist in the system and determines how this product should be distributed or "laid out" in a single predetermined manufacturing block (a certain processing equipment). Note also figure 11, in which product information (1103), equipment information (1104) and a manufacturing situation (1105) are stored in memory and that network (1108) is

connected to processing equipment (1110). See col. 8, lines 36-67. *The system of Kitamura, at the very least, implies that detection is occurring, otherwise, the system would not operate.*)

Both Blaimschein and Kitamura are considered to be analogous art because Blaimschein concerns a manufacturing process for cutting printed circuit boards and the like, and Kitamura concerns a manufacturing scheduling system for printed circuit board production systems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used the scheduling system of Kitamura with the production cutting placement system of Blaimschein so as to schedule parts for placement on sheets of material.

The suggestion/motivation would have been to schedule orders concerning cutting processes for printed circuit boards and verifying their completion. See abstract of Kitamura and Blaimschein, abstract.

Note further, that should parts of a particular group not fit on a single sheet, that it would have been obvious to place them on a further sheet that fit the part.

Therefore, it would have been obvious to combine Kitamura and Blaimschein in order to obtain the invention as described in Claim 1.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Turner. Turner discloses the following.

As described in Claim 1;

m. a schedule data storage unit (24) storing multiple manufacturing scheduling data including the kind of a printed wiring board scheduled to be manufactured and manufacturing quantity thereof;

n. a detecting unit (30) detecting a quantity of printed wiring boards which should be laid out in a single predetermined manufacturing block together with printed wiring boards of a different kind from multiple kinds of the printed wiring boards scheduled to be manufactured, according to multiple manufacturing data;

o. a condition data storage unit (32) storing a manufacturing condition data for laying out the printed wiring boards of different kinds in a single predetermined manufacturing block;

p. a dividing unit (22, 38, 40) dividing the detected quantity of printed wiring boards to multiple groups according to the manufacturing condition data;

q. a determining unit (22) determining a combination of the printed wiring boards of different kinds to be laid out in a single predetermined manufacturing block for each group. (see col. 7, lines 45-65 and col. 8, lines 1-58.)

Response to Arguments

10. Applicant's arguments filed 2/15/04 have been fully considered but they are not persuasive. See discussion above. Applicant asserts that there is no motivation to combine Kitamura and Kalagnanum. However, Kitamura describes a system for verifying process procedures in a manufacturing environment, said environment including the allocation of inventory, and Kalagnanum concerns an algorithm for matching inventory so as to reduce wasted material. Such a system of Kitamura in such an environment as a manufacturing inventory environment is considered to be concerned with efficiency and reduction of waste. Therefore, it would have been obvious for one ordinarily skilled in the art to look to Kalagnanum for a teaching of how to match inventory to orders so as to minimize waste. In addition, further rejections have been applied against Claim 1.

Applicant's representative is encouraged to contact the Examiner at the phone contact below, in order to discuss remaining issues in the case.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Blamschein '370, Susnjara '963, Beck '473, Lirov '508, Tadokoro '352, Surville '661, Herman, Jr., 275' and 444, Campestre '743, Scott 059', Lambert '458 are cited as examples of nesting systems.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey A. Shapiro whose telephone number is (703)308-3423. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald P. Walsh can be reached on (703)306-4173. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey A. Shapiro

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Examiner
Art Unit 3653

June 14, 2004